B.E. / B.Tech. (Electronics & Communication / Telecommunication Engineering) Model Curriculum Semester-III

SE103 / 003 - Digital System Design

P. Pages : 2 **GUG/W/24/13908**

Time : Three Hours * 5 5 2 0 * Max. Marks : 80

Notes : 1. All question carry marks as indicated.
2. Due credit will be given to neatness and adequate dimensions.
3. Assume suitable data wherever necessary.
4. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) Simplify $Y = AB + AB'C + BC'$ using Boolean algebra. **4**

b) Solve **4**

i) $(298)_{10} = (?)_{BCD}$

ii) $(57.35)_{10} = (?)_{8}$

c) Minimize using K-Map $F = \Sigma m(0,2,5,7,8,10,16,19,21,23,24,27,31)$ **8**

OR

2. a) Minimize using K-Map $F = \Pi M$ (4, 6, 10, 12, 13, 15) and implement using NOR only. **8**

b) Simplify the logic function $F(A,B,C) = \Pi M(3,5,6,11,13,14,15) + d(4,9,10)$ using K-map in SOP and POS form implement using basic gate. **8**

3. a) Draw 8:1 Mux using 2:1 Mux only. **4**

b) Implementing the Boolean function $F(A,B,C) = \Sigma m(2,4,7)$ using multiplexer such that MSB of the input variable is connected to input of multiplexer and remaining input to the select lines. **6**

c) Construct a full Subtractor circuit using a 3-to-8 line decoder and NOR gate. **6**

OR

4. a) Realize Full Adder using two half Adder, Write the Truth table and Output expression for Full adder. **8**

b) Design BCD to excess-3 code convertor. **8**

5. a) Convert D Flip Flop to SR Flip Flop. **6**

b) Design a Moore type sequence detector to detect the sequence 111 using JK flip flop. The detector accepts input as a string of bits either 0 or 1. Its output goes to 1 when a target sequence has been detected (Over lapping is allowed, Assum suitable input bits stream). **10**

OR

6. a) Explain about the various components of ASM chart. **6**

b) Construct asynchronous Up-Down counter using direction control. Show its waveform. **10**

7. a) Explain the operation of 2-Input TTL NAND gate. **8**

b) Design a PLA structure for the following function. **8**

$F1 = \Sigma m(0,1,2,3,4,7,8,11,12,15);$

$F2 = \Sigma m(2,3,6,7,8,9,12,13);$

$F3 = \Sigma m(1,3,7,8,11,12,15);$

$F4 = \Sigma m(0,1,4,8,11,12,15)$

OR

8. a) Compare CPLD and FPGA. **4**

b) Draw CMOS inverter? Explain its operation in brief. **6**

c) Explain the classification of memory. **6**

9. a) Describe the DSD Design Flow. **6**

b) Write a VHDL code for four input priority encoder using when else statement. **10**

OR

10. a) If A = "101", B = "011" and C = "010". What are the values of the following statements- **6**

i) (A & B) OR (B & C) ;

ii) A OR B and C

iii) (A & not B or C ror 2)

b) What are the different data types in VHDL explain giving example. **10**

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