B.E. / B.Tech. (Electrical (Electronics & Power) Engineering) Model Curriculum Semester-IV

SE202 - Digital Electronics

P. Pages : 2 **GUG/W/24/13804**

Time : Three Hours * 5 4 5 9 * Max. Marks : 80

Notes : 1. All questions carry marks as indicated.
2. Assume suitable data wherever necessary.
3. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) Simplify Y = AB' + (A'+B) C using Boolean algebra. **4**

b) Solve : **6**
i) (101.11011) 2 = (?) Decimal
ii) (345)10 = (?) Excess-3
iii) (11001)2 = (?) 2's complement

c) Prove NAND and NOR gate is a universal gate. **6**

OR

2. a) Subtract 4110 from 6810 using 1's compliment. **4**

b) State and Prove Distributive Law. **4**

c) Explain the operation of 2-Input TTL AND gate. **8**

3. a) Minimize using K-Map F= IIM (0, 1, 4, 6) **4**

b) Realize 16:1 Multiplexer using 4:1 Multiplexer only. **6**

c) Design 3-bit Grey to Binary code convector. **6**

OR

4. a) Design 4 bit BCD adder. **8**

b) Minimize the function using McClusky F = S (0, 1, 2, 8, 10, 11, 14, 15) **8**

5. a) Define Setup Time and Hold Time in Flip flop. **4**

b) Convert D flip flop to JK Flip Flop. **6**

c) Explain 4-bit SISO and SIPO shift register. **6**

OR

6. a) Explain JK Flip Flop give its Characteristic Table, Characteristic Equation and Excitation table. **8**

b) Design a Mod-6 synchronous counter using JK Flip Flop with separate logic circuitry for each J and K input. Construct a state to determine whether the counter is self starting or not? **8**

7. a) Explain the operation of Sample and hold circuit with diagram? Why Sample and hold circuit is used in ADC. **8**

b) Define resolution, accuracy, settling time and dynamic non linearity of DAC. **8**

OR

8. a) Write short note on 3 bit R-2R ladder DAC. **8**

b) Describe Successive approximation A/D convertor. **8**

9. a) Explain the classification and characteristic of memory. **8**

b) Draw and explain architecture of CPLD. **8**

OR

10. a) Design a PROM structure for the following function **8**
F1= Σ m (0, 1, 8, 11, 12, 15); F2 = Σ m (2, 3, 6, 7, 8, 9, 12, 13);
F3 = Σ m (1, 3, 7, 8, 11, 12, 15); F4 = Σ m (0, 1, 4, 8, 11, 12, 15).

b) Design a 2-bit comparator using PLA. **8**

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