B.E. / B.Tech. Computer Science & Engineering (Model Curriculum) - Semester-III

SE104CS - Digital Electronics

P. Pages : 2 **GUG/W/24/13804N**

Time : Three Hours * 7 4 7 8 * Max. Marks : 80

Notes : 1. All questions carry marks as indicated.
2. Assume suitable data wherever necessary.
3. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) State and Prove Absorption Law. **4**

b) Convert the following: **6**
i) $(101010.01)2 = (?)$ 2's complement
ii) $(3267)10 = (?)$ 9's complement
iii) $(345)10 = (?)$ Excess-3

c) Implement EXOR gate using NOR gate only. **6**

OR

2. a) Solve: **4**
i) $1011+1101+1001+111=?$
ii) $1001.01-1111.11=?$

b) Simplify Y = (B + BC) (B + B'C) (B + D) using Boolean algebra. **4**

c) Draw CMOS NAND and NOR gate and explain its operation. **8**

3. a) Simplify the logic function $F(A,B,C,D) = \Sigma m(0,1,2,5,6,8) + d(3,4,7,14)$ using K-map in SOP and POS form implement using basic gate. **8**

b) Realize 4-bit BCD adder. **8**

OR

4. a) Design 1-bit magnitude comparator. **4**

b) Draw 8 : 1 Multiplexer using 2:1 Multiplexer only. **6**

c) Implement even parity generator for a 3-bit binary message. **6**

5. a) What is race around condition in JK Flip-Flop? How it can be avoided. **4**

b) Convert T flip flop to D Flip Flop. **6**

c) Elaborate 3-bit Ring counter with its waveform. **6**

OR

6.	a)	Explain 4-bit SISO and PISO shift register with diagram and waveform.	**6**
	b)	Design 3-bit Up-Down counter with direction control M using JK flip-flop such that when m=0 counter should count upward else downward.	**10**
7.	a)	Explain the counter type ADC with suitable diagram. What are the limitations of this convertor?	**8**
	b)	What is DAC? Draw the n-bit binary weighted DAC and explain its operation.	**8**

OR

8.	a)	What is DAC? Write few applications of DAC.	**6**
	b)	Compare Flash, Dual slope and Successive approximation type ADC.	**10**
9.	a)	Discuss the classification of memory.	**4**
	b)	Compare PROM, EPROM & EEPROM.	**4**
	c)	Design a PLA structure for the following function $F1 = \Sigma m(0,1,2,3,4,7,8,11,12,15)$; $F2 = \Sigma m(2,3,6,7,8,9,12,13)$; $F3 = \Sigma m(1,3,7,8,11,12,15)$; $F4 = \Sigma m(0,1,4,8,11,12,15)$.	**8**

OR

10.	a)	Design a 2-bit comparator using PROM.	**8**
	b)	What is CPLD? Explain the operation of CPLD with a suitable diagram.	**8**

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