B.E. Electronics & Communication / Telecommunication Engineering (Model Curriculum)
Semester-VI

ET601M3 - Program Elective-II - CMOS Design

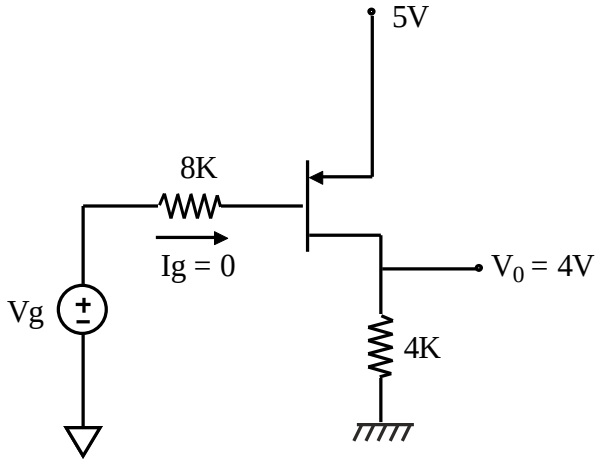
P. Pages : 2 **GUG/W/24/13930**

Time : Three Hours * 5 5 4 2 * Max. Marks : 80

Notes : 1. All questions carry marks as indicated.
2. Assume suitable data wherever necessary.
3. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) Define Channel length modulation? Derive an expression for I_{DSAT} and channel length modulation coefficient. **8**

b) For the PMOS circuit shown in figure. Find the value of I_D and V_{DS}. **8**



OR

2. a) Differentiate between NMOS and PMOS. **4**

b) Elaborate the action of enhancement type MOSFET in (i) Linear region (ii) Cut off region (iii) Saturation region. **6**

c) With the help of following parameters determine in which region MOSFET is working and find the value of drain current I_D. **6**

$V_{TN} = 0.8$, $\lambda = 0.04V^{-1}$, $Kn' = 20\ \mu A / v^2$, $W / L = 20$, $V_D = 4\,V$, $V_G = 5V$ and $V_S = 2V$

3. a) Summarize the Czochralski process of Wafer formation for the production of ingot seed with the help of neat diagram. **8**

b) Explain fabrication of CMOS by N-well process. **8**

OR

4. a) Write a short note on Re crystallization technique. **4**

b) Consider a CMOS inverter circuit with following parameters; **12**
$V_{DD} = 3.3V$; $V_{IN} = 0.6V$; $V_{TP} = -0.7V$; $Kn = 200\mu A / V^2$; $Kp = 80\mu A / V^2$;
Calculate the Noise margin of the circuit.

5. a) What is delay? Explain. How it is calculated. **8**

b) Derive an expression for short circuit dissipation for CMOS. **8**

OR

6. a) How transistor scaling is done? Discuss its effect. **8**

b) What is Logical effort? State its limitation. **8**

7. a) Design 2:1 MUX using CMOS. **6**

b) Design AND gate and NOT gate with the use of stick diagram and physical layout structure. **10**

OR

8. Design a CMOS logic circuit for the following Boolean functions. **16**

i) $Z = \overline{A.(D+E)+B.C}$

ii) $Z = \overline{(A+B+C+D)}$

iii) $Z = \overline{(A.B+C.(A+B))}$

9. a) Describe the dual edge triggered flip-flop. **8**

b) Describe static sequential circuit. **8**

OR

10. a) Design CMOS positive edge triggered D-register.. **8**

b) Design CMOS S-R Latch by using NOR gate and NAND gate. **8**

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