M.Sc. F.Y. (Electronics) (NEP Pattern) Semester-I

NEP-32 / PSCELT102 - Paper-II : Analog and Digital System

P. Pages : 2 **GUG/W/24/15088**

Time : Three Hours * 5 9 7 1 * Max. Marks : 80

Notes : 1. All questions are compulsory and carry equal marks.
2. Draw neat and label diagram wherever necessary.

Either:

1. a) Draw the circuit diagram of two stages RC coupled transistor amplifier. Explain its working. **8**

b) What is FET amplifier? Explain construction and working of FET amplifier. **8**

OR

c) What is multistage amplifier? Explain working and application multistage amplifier. **8**

d) What is current mirror circuit? Explain its specification and limitation. **8**

Either:

2. a) Explain block diagram of Phase Lock Loop (PLL). **8**

b) Explain OPAMP as Wave-Shaping circuit. **8**

OR

c) State differences between oscillator and amplifier. Explain the construction and working of Schmitt trigger circuit. **8**

d) Explain application of OPAMP as an **8**
i) Integrator ii) Differentiator

Either:

3. a) Explain 4x4 keyboard encoder. **8**

b) Draw the state diagram of a DFF and obtained its characteristics equation. Draw the timing diagram. **8**

OR

c) What is decoder? Describe working of 4-bit binary decoder. **8**

d) Compare the Mealy and Moore Models using typical state diagram. **8**

Either:

4. a) What is CPLD? Draw and explain the black diagram of CPLD. **8**

b) What is FPGA? Draw its block diagram and explain. **8**

OR

c) Discuss the architecture of Programmable Logic Array (PLA). **8**

d) Discuss architecture of ROM in details. **8**

5. Solve the following.

a) Explain frequency response of multistage amplifier and define bandwidth. **4**

b) What is frequency to voltage converts? Explain. **4**

c) Explain difference between decoder and demultiplexer. **4**

d) Describe the methods of packaging of CPLDs. **4**

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