B.E. Electronics & Communication / Telecommunication Engineering (Model Curriculum)
Semester - III

003 - Digital System Design

P. Pages : 2 **GUG/S/23/13908**

* 2 6 4 5 *

Time : Three Hours Max. Marks : 80

Notes : 1. All questions carry marks as indicated.
2. Assume suitable data wherever necessary.
3. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) Solve **4**

i) $(1762.46)_8 = (?)_{16}$

ii) $(127.25)_{10} = (?)_2$

b) Perform following subtraction using is 1's complement. **4**

i) 100101 – 10011 ii) 11100 – 00100

c) Simplify **8**

i) $A+B+C+D+\overline{ABCD}$ ii) $AB+A\bar{B}C+A\bar{B}\bar{C}$

OR

2. a) Simplify the Boolean function using k - map. **8**
$f = \sum m(2,3,6,7,10,11,12)$ in SAP and POS form. Implement using logic gate.

b) Simplify **8**

i) $\left(AB\left(C+\overline{BD}\right)+\overline{AB}\right)CD$ ii) $\overline{(A+BC)\left(\bar{A}\bar{B}+C\right)}$

3. a) Define Multiplexer? Implement the following function using 8:1 multiplexer with LSB connected to select line & multiplexer. **8**
$f(AB\ CD) = \sum m(1,3,4,11,12,13,14,15)$

b) Design full adder using NAND gate only. **8**

OR

4. a) Design BCD to 7 - segment decoder with active high output connected to common cathode type display. **8**

b) Design a 2 - bit magnitude comparator circuit. **8**

5. a) What is Race around condition? Explain in brief the solution to overcome race - around condition. **8**

b) Design a Mealy's type serial adder with state diagram, state table, value assigned state table, output expression and block diagram. **8**

OR

6. a) Convert D flip flop to SR flip flop. **6**

b) Design a 3 - bit up/down counter using JK flip flop with direction control M. The counter counts upward for M = 0 and counts downward for M = 1. **10**

7. a) What is PLA? Implement for following function using PLA. **8**

$F_1(ABC) = \sum m(0,1,2,4)$

$F_2(ABC) = \sum m(0,5,6,7)$

b) A quad two input AND gate has following parameter **8**

$V_{OH(min)} = 2.7V$

$V_{OL(max)} = 0.4V$

$V_{IH(min)} = 2V$

$V_{IL(max)} = 0.8V$

$I_{CCH} = 18\,mA$

$I_{CCL} = 32\,mA$

$\lambda_{PLH} = 4.5\,ns$

$\lambda_{PHL} = 5.0\,ns$

Determine the speed - power product and noise margin.

OR

8. a) Realize the following function using a PAL. **9**

$F_1(ABCD) = \sum m(6,8,9,12,13,14,15)$

$F_2(ABCD) = \sum m(1,4,5,6,7,10,11,12,13)$

$F_3(ABCD) = \sum m(4,5,6,7,10,11)$

$F_4(ABCD) = \sum m(4,5,6,7,9,10,11,12,13,14,15)$

b) Write short note on characteristics of digital IC's. **7**

9. a) Compare signals and variables. **4**

b) What are the different types and operators of VHDL? Explain with one example each. **12**

OR

10. a) Compare synthesis and simulation. **4**

b) Differentiate VHDL and Verilog. **4**

c) Explain the behavioral modeling style in VHDL. Write a behavioral VHDL code of 2-input AND gate. **8**

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