B.E. Computer Science & Engineering (Model Curriculum) Semester - III

SE103CS - Computer Architecture and Organization

P. Pages : 2 **GUG/S/23/13803**

Time : Three Hours * 2 5 4 0 * Max. Marks : 80

Notes : 1. All questions are compulsory.
2. All questions carry equal marks.
3. Due credit will be given to neatness and adequate dimensions.
4. Assume suitable data wherever necessary.

1. a) Define the term addressing modes and explain the different addressing modes with suitable diagram and example. **8**

b) Write a short note on bus structure. **8**

OR

2. a) Explain the role of stack in subroutine call implementation with example. **8**

b) Explain functional units of basic computer system. **8**

3. a) What is the control sequence for execution of the instruction. **8**
Add R_1, R_2

b) What is 3-bus organization of CPU? Explain in detail how data transfer takes place between two registers. **8**

OR

4. a) Explain in brief Hardwired control unit organization. **8**

b) Write steps for execution of complete instruction. Explain with SUB instruction. **8**

5. a) Explain prefetching of micro instruction and Emulation. **8**

b) With a neat sketch explain Bit slice. **8**

OR

6. a) With a neat sketch explain micro instruction with next address field. **8**

b) Write and explain micro routine for Branch < 0. **8**

7. a) Explain Booth's algorithm with diagram. **8**
Multiply the following number using booth's algorithm.
-19×14

b) Multiply using Bit recoding of multiplier method. **8**
$(+42) * (-7)$

OR

8. a) Express $4 \cdot 772 \times 10^3$ in IEEE single precision and double precision floating point format. **8**

b) Multiply using Bit pair recoding of multiplier method. **8**
$(+13) \times (-6)$

9. a) Write in detail cache memory and its need. **8**

b) Design $2M \times 32$ memory module using $512k \times 8$ static memory chips. **8**

OR

10. a) Explain Virtual Memory Address Translation with a neat sketch. **8**

b) Explain set Associative Mapping function of cache memory. **8**

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