B.E. Electronics & Communication/Telecommunication Engineering (Model Curriculum)
Semester - VI

ET601M3 - Program Elective-II : CMOS Design

P. Pages : 2 **GUG/S/23/13930**

Time : Three Hours * 2 6 6 7 * Max. Marks : 80

Notes : 1. All questions carry as indicated marks.
2. Assume suitable data wherever necessary.
3. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) Determine the history of CMOS circuit. **2**

b) Explain : **6**
i) Body effect ii) Short channel effect.

c) Explain the N-channel enhancement type MOSFET along with its input and output characteristic. **8**

OR

2. a) Write a note on IC technology. **4**

b) Elaborate the action of enhancement type MOSFET for different values of Vgs. **6**

c) Identify in which region MOSFET is working and also find the value of aspect ratio (W/L) for the below mentioned parameters $V_{TN} = 0.8$, $\lambda = 0.05V^{-1}$, $\mu_n C_{ox} = 20\mu A / v^2$, $I_D = 0.24mA, V_D = 5V, V_G = 2.8V$ and $V_S = 1V$. **6**

3. a) Discuss in detail about following technique used in producing silicon-on-insulator technology. **8**
i) Hetro-epitaxial technique
ii) Homo-epitaxial technique
iii) Re crystallization technique

b) Obtain the DC transfer characteristic of CMOS inverter and mark all the regions showing the status of NMOS and PMOS. **8**

OR

4. a) Write a short note on Beta-ratio effect. **4**

b) Consider a CMOS inverter circuit with following parameters; **12**
$V_{DD} = 5V : V_{Tn} = 0.6V; V_{Tp} = -0.7V; Kn = 200\mu A / V^2; Kp = 110\mu A / V 2;$
Calculate the Noise margin of the circuit with Kr = 1.81.

5. a) What is latch up problem in CMOS? Draw and explain its physical origin and V-I characteristic. **8**

b) Write a short note on:- **8**
i) RC delay model
ii) Linear delay model.

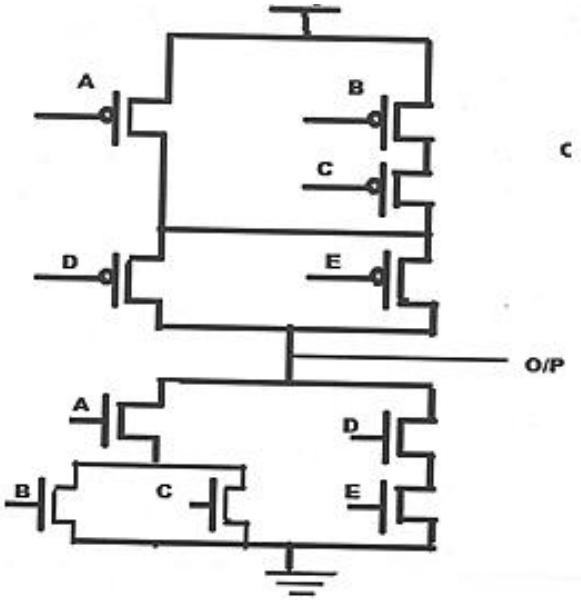
OR

6. a) What are the three types of power dissipation in CMOS logic circuit? Derive an expression for total power dissipation. **8**

b) Write a short note on: **8**
i) Logical efforte
ii) Parasitic delay

7. a) Explain complementary pass transistor logic. **6**

b) For the given CMOS circuit draw stick diagram and physical layout using Euler's graph. **10**



OR

8. a) Write a short note on **8**
i) Domino Logic
ii) NORA logic

b) Design the following combinational circuit. **8**
i) CMOS Half adder
ii) CMOS Half subtractor

9. a) Explain in detail conventional CMOS flip-flops. **8**

b) Describe static sequential circuit. **8**

OR

10. a) Describe enabled latches and flip-flop in detail. **8**

b) Design CMOS S-R flip flop by using NOR gate and NAND gate. **8**

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