B.E. Computer Science & Engineering (Model Curriculum) Semester - III

SE104CS - Digital Electronics

P. Pages : 2 **GUG/S/23/13804N**

Time : Three Hours * 2 5 4 1 * Max. Marks : 80

Notes : 1. All questions carry marks as indicated.
2. Assume suitable data wherever necessary.
3. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) Solve the following. **8**

i) $(11010101)_B = (\ ?\ )_G$

ii) $(110101 \cdot 100)_2 = (\ ?\ )_D$

iii) $(19 \cdot 125)_{10} = (\ ?\ )_B$

iv) $(24)_{10} = (\ ?\ )_5$

b) Explain 3-input CMOS NAND gate. **8**

OR

2. a) Encode the data bits 0011 into 7-bit even parity hamming code. **4**

b) Write short note on **6**
i) ASCII Code ii) EBCDIC Code

c) What is even parity and odd parity scheme? In even parity scheme, which of the following word contain error **6**
i) 10011010 ii) 10111001

3. a) Define Decoder? Implement a Full Adder using 3 to 8 decoder. **8**

b) Design a BCD to excess-3 code convertor. **8**

OR

4. a) Implement 4-bit priority encoder with input D_0, D_1, D_2 and D_3, of which D_3 is having the highest priority. **8**

b) Solve using K-map and implement using basic gate **8**
$f = \Sigma m(0,1,2,3,6,7,13,15)$.

5. a) Differentiate between combinational and sequential circuit. **4**

b) Design a 3-bit Up/Down counter using control signal M. For M=0 the counter counts upward. For M=1 the counter counts downward. Draw its waveform. **12**

OR

6. a) Convert JK Flip Flop to SR Flip Flop. **8**

b) Explain **8**
i) Serial in serial out
ii) Parallel in Parallel out
shift register.

7. a) Write a short note on Dual slope type Analog to Digital convertor. **8**

b) Explain successive approximation type Analog to Digital convertor. **8**

OR

8. a) Explain different specification parameters of Analog to Digital convertor. **8**

b) Explain R-2R ladder type Digital to Analog convertor. **8**

9. a) Explain memory organization with its operation. **8**

b) What is programmable Logic Array? Implement the following boolean function with a PLA **8**
i) $F_1(A, B, C) = \Sigma m(0, 1, 2, 4)$
ii) $F_2(A, B, C) = \Sigma m(0, 5, 6, 7)$

OR

10. Write short note on. **16**

i) Expansion of memory size.

ii) Content Addressable memory.

iii) CPLD.

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