

M.Sc. F.Y. (Electronics) (CBCS Pattern) Semester - I  
**PSCELET02 - Paper-II : Digital Design & Applications**

P. Pages : 2

Time : Three Hours



**GUG/S/23/11155**

Max. Marks : 80

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- Notes : 1. All questions are compulsory and carry equal marks.  
2. Draw well labeled diagrams wherever necessary.

**Either:**

1. a) What is the K - map method to simplify any Boolean function? What are the advantages and disadvantages of using the Karnaugh map? **8**
- b) What is two - level NAND gate? Simplify the following functions and Implement them with two - level NAND gate? **8**

**OR**

- c) What is a multiplexer? What are the advantages of using multiplexer? Explain the procedure of combinational logic design using multiplexers. **8**
- d) What is a decoder? Explain BCD - to - Decimal decoder using gates. **8**

**Either:**

2. a) Define a flip - flop. Explain the wording of RS flip - flop using NAND or NOR gates. Write truth table. **8**
- b) Explain the working of J - K flip - flop. Draw logic diagram of J - K master slave flip - flop and explain its truth table? **8**

**OR**

- c) With the help of a block (logic) diagram, explain the working of a ripple Counter. Write its truth table. Differentiate between synchronous and Asynchronous counters. **8**
- d) Write a note on up - down counters. Explain the working of ring counter using D flip - flops. Draw the waveforms? **8**

**Either:**

3. a) Explain Half adder and full adder with logic diagram, equations, truth table and using gates. Write equations for carry and sum. **8**
- b) Write a note on 4 - bit binary adder and binary adder - subtractor. **8**

**OR**

- c) What is a demultiplexer (DEMUX)? State the uses of demultiplexers. Draw logic diagram of 1:4 demultiplexer and explain its working. **8**

- d) What is an ALU? How does an arithmetic - logic unit work? What type of functions do ALUs support? **8**

**Either:**

4. a) What is VHDL Architecture? Define with example, the following terms related to VHDL. **8**  
i) Entity ii) Architecture  
iii) Configuration iv) Package
- b) What do you mean by ROM? How to write simple ROM in VHDL? **8**

**OR**

- c) What do you mean by PLA draw its block diagram and explain its working? **8**
- d) What is a CPLD? Explain architecture of complex programmable logic device with applications? **8**

5. Attempt the following.

- a) Implement the following multi - output combinational logic circuit using a 4 - to - 16 - line decoder. **4**  
 $F1 = \sum m(2, 3, 6, 9, 12, 15)$   
 $F2 = \sum m(2, 4, 6, 8, 10, 12, 14)$   
 $F3 = \sum m(4, 8, 12)$   
 $F4 = \sum m(5, 10, 15)$
- b) Explain Mealy and Moore Models with examples? **4**
- c) What is shift register explain in details? **4**
- d) Explain different types of operators in VHDL? **4**

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