B.E. Electronics & Communication/Telecommunication Engineering (Model Curriculum) Sem-III

003 : Digital System Design

P. Pages : 2 **GUG/W/22/13908**

Time : Three Hours * 3 1 3 7 * Max. Marks : 80

Notes : 1. All questions carry marks as mentioned.
2. Due credit will be given to neatness and adequate dimensions.
3. Assume suitable data wherever necessary.
4. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) Simplify F(A,B,C) = AB+AB'C+AB'C' using Boolean algebra. **4**

b) Solve **4**
i) $(101010.01)_2 = (?)_{2\text{'s complement}}$
ii) $(19.125)_{10} = (?)_2$

c) Realize y= (AB + BC)C using 2-input NAND gate only. **8**

OR

2. a) Solve **2**
$(345)_{10} = (?)_{\text{Excess}-3}$

b) Minimize using K-Map F= Π M (0, 4, 7). d(1, 2, 6). **6**

c) Simplify the logic function F(A, B, C) $= \Sigma m(0,1,3,5)$ + d(2, 7) using K-map in SOP and POS form implement using basic gate. **8**

3. a) Design Half Subtractor with Truth Table, K-map for Difference and Borrow? **4**

b) Implement the Boolean function $F(A,B,C) = \Sigma m(2,4,7)$ using multiplexer such that LSB of the input variable is connected to input of multiplexer and remaining input to the select lines. **6**

c) Realize half adder using 2:1 Mux. **6**

OR

4. a) Design BCD to 7-segment decoder (assume common Anode). **8**

b) Design 3-bit Gray to Binary code convertor. **8**

5. a) Draw the state diagram of D Flip Flop. **4**

b) What is an ASM chart? Explain with an example. **4**

c) Design 3-bit Up-Down counter with direction control M using JK flip-flop such that when m=0 counter should count upward else downward. **8**

OR

6.	a)	Convert D flip flop to T flip flop.	**6**
	b)	Design a Moore's type sequence detector to detect the sequence 111 using JK flip flop (over lapping is allowed). The detector accepts input w as a string of bits. w can be either 0 or 1. Its output goes to z=1 when a target sequence has been detected else z=0. (Assume random input sequence to verify the output)	**10**
7.	a)	Explain CMOS Ex-OR gate?	**4**
	b)	Calculate Noise Margin for given $V_{ILmax} = 0.8V$, $V_{IHmin} = 2.0V$, $V_{OLmax} = 0.4V$ and $V_{OHmin} = 2.4V$	**4**
	c)	Design Full Adder using PLA.	**8**

OR

8.	a)	Draw and explain the architecture of a FPGA? Explain with example how LUTs are configured to implement a design.	**8**
	b)	Define the following terms Fan in, Fan out, Propagation delay, Noise margin, power dissipation, speed of operation, Cost.	**8**
9.	a)	Discuss about variable assignments with examples in VHDL.	**4**
	b)	Explain the different types of operators in VHDL.	**6**
	c)	Discuss about signal assignments with examples in VHDL.	**6**

OR

10.	a)	Compare Signals and Variables.	**6**
	b)	If A = "10110111", compute the following; i) A SLL 2; ii) A SRL 3; iii) A SLA 3; iv) A SRA 2; v) A ROL 3;	**10**

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