B.E. Electronics & Communication/Telecommunication Engineering (Model Curriculum) Sem-VI

ET601M3 : Program Elective-II : CMOS Design

P. Pages : 2 **GUG/W/22/13930**

Time : Three Hours * 3 1 5 9 * Max. Marks : 80

Notes : 1. All questions carry marks as indicated.
2. Due credit will be given to neatness and adequate dimensions.
3. Assume suitable data wherever necessary.
4. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) Compare NMOS and PMOS. (minimum 8 points) **4**

b) With the help of following parameters determine in which region MOSFET is working and also find the value of drain current I_D. **4**

$V_{TN} = 0.8, \lambda = 0.04V^{-1}, Kn' = 20\mu A / v^2, W/L = 20,\ V_D = 4V, V_G = 5V$ and $V_S = 2V$.

c) Explain the working of NMOS Enhancement transistor along with its input and output characteristics. **8**

OR

2. a) How does MOS transistor acts as a switch? **4**

b) Explain the following term **12**
i) Chanel length modulation
ii) Body effect
iii) Threshold voltage

3. a) Explain the operation of Bi - CMOS Inverter. **4**

b) Summarize the fabrication of IC with respect to Oxidation, Etching, Photolithography, Ion Implantation. **4**

c) Differentiate between $\lambda-$ based design rules and $\mu-$based design rules. **4**

d) Design CMOS inverter with the help of stick diagram and physical layout. (use λ based design rules) **4**

OR

4. Derive an expression for CMOS inverter. **16**
i) Low input voltage V_{IL}.
ii) High input voltage V_{IH}.
iii) Low output voltage V_{OL}.
iv) High output voltage V_{OH}.

5. a) What is delay? Explain. How it calculated. **8**

b) Write a short note on: - **8**

i) Logical efforts

ii) Parasitic delay

OR

6. a) Derive an expression for short circuit dissipation for CMOS. **8**

b) Write a short note on: - **8**

i) Resistance estimation

ii) Capacitance estimation

7. Design a CMOS logic circuit for the following Boolean functions. **16**

i) $Y = A.(B + C) + CD$

ii) $Y = \overline{(A + B + C + D)}$

iii) $Y = \overline{(A.B + C.(A + B))}$

iv) $Y = (A + B).C + D$

OR

8. a) Differentiate between static and dynamic CMOS. **4**

b) Design two universal gate by using CMOS along with its stick diagram and physical layout. (for drawing physical layout use λ based design rules) **12**

9. a) Design the following sequential CMOS circuits. **8**

i) S-R flip - flop

ii) J-K flip - flop

b) Explain in detail dual edge triggered flip - flop. **8**

OR

10. a) Write short note on static sequential circuits. **4**

b) Design CMOS positive edge triggered D - register. **6**

c) Explain in detail conventional CMOS latches. **8**

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