M.Sc. F.Y. (Electronics) (CBCS Pattern) Sem-I

PSCELET02 / PSELT102 - Paper-II : Digital Design & Applications

P. Pages : 2 **GUG/W/22/11155**

Time : Three Hours *1909* Max. Marks : 80

Notes : 1. All questions are compulsory and carry equal marks.
2. Draw neat diagram and truth table wherever necessary
3. Use of log table / Calculator is allowed.

Either:

1. a) Design the circuit that implements the Boolean function, $f(A,B,C)=\sum m(2,3,5,7)$, using NAND gates only. **8**

b) Implement the following function using an 8:1 MUX. **8**
$y(A,B,C,D)=\sum m(0,3,4,8,9,15)$

OR

c) A CMOS gate is connected at V_{DD} =9V and it is driven by a standard TTL gate. Explain their interfacing. **8**

d) Explain the difference between Open – Collector and totem – pole outputs. **8**

Either:

2. a) Draw the state diagram of a JKFF and obtain its characteristic equation Draw its timing diagram. **8**

b) Explain the difference between synchronous and asynchronous counters design a mod – 3 ripple counter using TFFs. Draw its timing diagrams. **8**

OR

c) What is lockout condition of a counter? Explain how lockout condition is prevented in synchronous counters. **8**

d) Compare the mealy and Moore models using typical state diagrams. **8**

Either:

3. a) Write a VHDL Program for the 4:1 MUX using the behavioral modeling. Draw the simulation waveforms **8**

b) Explain the following VHDL terms: **8**
i) Entity
ii) Package
iii) Generic

OR

c) Write a VHDL program for a full adder circuit. Draw the simulation waveforms. **8**

d) Explain the data flow modeling in VHDL. Write the entity to construct the R-S flip – flop with input ports SET and RESET. **8**

Either:

4. a) Describe the internal architecture of a CPLD. Explain the working of a typical microcell. **8**

b) Explain the architecture of basic FPGA. **8**

OR

c) Discuss the architecture of Programmable Logic Array (PLA). **8**

d) Explain the architectures of ROM **8**

5. a) Explain the function of a tristate TTL inverter. **4**

b) Draw the Moore state diagram for the following input – output bit sequence. **4**
input W = 0 1 1 0 1
output Z = 0 0 0 1 0

c) Explain the structural modeling in VHDL with an example. **4**

d) Explain the methods of packaging of CPLD. **4**

****