

B.Tech. / B.E. Electronics & Communication/Telecommunication Engineering (Model Curriculum)  
Semester-III  
**103 / 003 - Digital System Design**

P. Pages : 2

Time : Three Hours



**GUG/W/23/13908**

Max. Marks : 80

- Notes :
1. All questions carry marks as indicated.
  2. Assume suitable data wherever necessary.
  3. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) Convert the given equation into standard canonical SOP form  $f = AC + AC' + B'C$ . **4**
- b) Solve **4**
- i)  $(0.6875)_{10} = (?)_2$  ii)  $(4021.2)_5 = (?)_{10}$
- c) Minimize using K-Map  $f(W, X, Y, Z) = \Pi M(0, 1, 2, 3, 4, 5, 6, 7, 10, 11)$ . **8**

**OR**

2. a) Minimize using K-map and realize using NAND gate only **8**  
 $F = AB + AC' + C + AD + AB'C + ABC$
- b) Simplify the logic function  $F(A, B, C, D) = \Sigma m(0, 1, 2, 5, 6, 8) + d(3, 4, 7, 14)$  using K-map in SOP and POS form implement using basic gate. **8**
3. a) Draw 8:1 Multiplexer using 2:1 Multiplexer only. **4**
- b) Design 3-bit Binary to Gray code convertor. **6**
- c) Realize half adder using 2:1 mux. **6**

**OR**

4. a) Design 2-bit magnitude comparator. **8**
- b) Design 4 bit BCD adder **8**
5. a) What is an ASM chart? Explain with an example. **4**
- b) What is race around condition explain in detail. **4**
- c) Design a sequence generator that generates the sequence "100010011010111" **8**

**OR**

6. a) Convert T flip flop to JK flip flop. **6**
- b) Design a type T counter that goes through states 3, 4, 2, 1, 3, ----- . Is the counter self starting? **10**

7. a) Compare CPLD and FPGA? **4**
- b) Draw and explain the architecture of a FPGA. **6**
- c) Draw CMOS inverter? Explain its operation in brief. **6**

**OR**

8. a) Define the following terms Fan in, Fan out, Propagation delay, Noise margin, power dissipation, speed of operation, Cost. **8**
- b) Design a Full Subtractor using PLA and PAL. **8**
9. a) Elucidate the different types of operators in VHDL. **6**
- b) Write VHDL code for OR gate using case statement. **10**

**OR**

10. a) What are the different data types in VHDL explain giving example. **10**
- b) If A = "110", B = "111", C = "011000" and D = "111011", compute the following (A & not B or C or 2 and D) **6**

\*\*\*\*\*