B.E. Electrical (Electronics & Power) Engineering (Model Curriculum) Sem-IV
SE202 - Digital Electronics

P. Pages : 2   **GUG/W/23/13804**

Time : Three Hours   ‖‖‖‖‖‖‖‖   Max. Marks : 80
                                      * 7 3 9 1 *

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Notes : 1. All questions carry marks as indicated.
         2. Assume suitable data wherever necessary.
         3. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) Solve using Boolean algebra f = ABC + BC'D + A'BC   **4**

        b) Convert the following into octal.   **6**
            $(0.513)_{10}$

            $(123.CBD)_{16}$

            $(1100.101)_{10}$

        c) Explain NAND and NOR gate as universal gate.   **6**

                                      OR

2. a) Subtract 4110 from 6810 using 1's complement method.   **4**

        b) Explain the logic gates with truth tables.   **6**

        c) Explain CMOS NOR gate.   **6**

3. a) Solve using K-Map f (x, y, z) = m (0, 2, 4, 5, 6)   **4**

        b) Minimize using K-Map F = IIM (0, 6, 9, 10, 13). d (1, 3, 8)   **6**

        c) Realize Full Subtractor using two half adder.   **6**

                                      OR

4. a) What is a multiplexer? Explain 8:1 Multiplexer.   **8**

        b) Minimize the function using Quine McClusky F = S(1, 2, 5, 6, 7, 9, 10, 11, 14)   **8**

5. a) Explain Preset and Clear in Flip Flop.   **4**

        b) Design JK Flip Flop using D Flip Flop.   **6**

        c) Explain 3-bit ring counter.   **6**

                                      OR

6.	a)	Design a MOD-10 Asynchronous counter using T-flip flop.	**8**
	b)	Explain SISO, PISO, SIPO shift register.	**8**
7.	a)	What are the performance specification of ADC.	**8**
	b)	What is DAC? Explain binary weighted resister type DAC.	**8**

<div align="center">OR</div>

8.	a)	Explain flash type ADC with its advantage and disadvantages.	**8**
	b)	Explain 3 bit R-2R ladder DAC.	**8**
9.	a)	Draw and explain the architecture of a FPGA? Explain with example how LUTs are configured to implement a design.	**8**
	b)	Draw and explain architecture of CPLD.	**8**

<div align="center">OR</div>

10.	a)	Design full adder using PLA.	**8**
	b)	Write short note on . i) CCD ii) CAM	**8**

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