B.E. Electronics & Communication/Telecommunication Engineering (Model Curriculum)
Semester-VIII

ET803M - Advance Computer Architecture

P. Pages : 2 **GUG/W/23/14356**

Time : Three Hours * 7 8 9 5 * Max. Marks : 80

Notes : 1. All questions are compulsory.
2. All questions carry equal marks.
3. Due credit will be given to neatness and adequate dimensions.
4. Assume suitable data wherever necessary.
5. Diagram should be given wherever necessary.
6. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) State and explain the 4-stage instruction cycle. **8**

b) Differentiate between sequential and Parallel computing. **8**

OR

2. a) Analyze the need of Amdahl's Law. **7**

b) Write note on following. **9**

i) Single accumulator organization.

ii) General register organization.

iii) Stack organization.

3. a) Explain the 5-stage pipeline for a RISC processor. **8**

b) Explain why pipeline is hard to implement. **8**

OR

4. a) Explain how pipeline hazards are classified in brief. **8**

b) Write short note on static branch prediction technique. **8**

5. a) State and explain how Tomasulo algorithm works. **8**

b) What is super pipelining? Explain the pipeline structure and performance of the MIPS? **8**

OR

6. a) What is Multithreading? Explain its benefits. **8**

b) Explain very long instruction word (VLIW) architecture with its features. **8**

7. Write a short note on:

a) Write through and write back in cache. **8**

b) Average memory access time (AMAT). **8**

OR

8. a) Explain cache replacement algorithms in detail. **16**

9. a) Write a short on Tiled chip multicore processors (TCMP). **8**

b) What is topology in computer architecture? What needs to be considered when designing topologies? **8**

OR

10. a) What is Crossbar switch in computer architecture? **8**

b) Explain Input/Output- buffered router architecture model with pipeline stages. **8**

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