B.E. Electronics & Communication/Telecommunication Engineering
(Model Curriculum) Semester-V
ET503M - Computer Architecture

P. Pages : 2
Time : Three Hours

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Max. Marks : 80

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Notes :
1. All questions are compulsory.
2. All questions carry equal marks.
3. Assume suitable data wherever necessary.

1. a) What is Register level components? Explain with general block representation. **8**

b) How description language are used to describe the structure and behavior of any system. **8**

OR

2. a) What are different levels of design in a computer system. Compare the different levels of design. **8**

b) Explain prototype structure and performance measurement of processor level design. **8**

3. a) Multiply 13 * 5 by using Booth Algorithm? **8**

b) Write a short note on instruction format. **8**

OR

4. a) Draw the internal architecture of a typical CPU with general registers and explain, the functional part of CPU in brief. **8**

b) Explain IEEE754 single and double precision formal. **8**

5. a) Explain micro programmed control unit in detail. **8**

b) Explain in detail Hardwired control unit with the help of neat labelled diagram. **8**

OR

6. a) Write a short note on Emulation. **8**

b) What is meant by Micro program sequencer? Explain with block diagram. **8**

7. a) What is need of memory management? Explain memory management techniques in brief. **8**

b) Write short note on various page replacement algorithm also explain with example. **8**

OR

8.	a)	Explain in detail, the organization of 64k*8 memory Module using 16*1. With suitable block diagram.	**8**
	b)	Explain ROM Memories and its types.	**8**
9.	a)	What is instruction pipelining? Explain with block diagram of 4 stage pipeline.	**8**
	b)	Write short note on-	**8**

        i)   CPU Control unit.

        ii)   Interconnected network.

<div align="center">OR</div>

10.	a)	Explain how pipeline influences on instruction set design.	**8**
	b)	Write short note on Hazards.	**8**

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