B.E. Electronics & Communication/Telecommunication Engineering (Model Curriculum)
Semester-VI
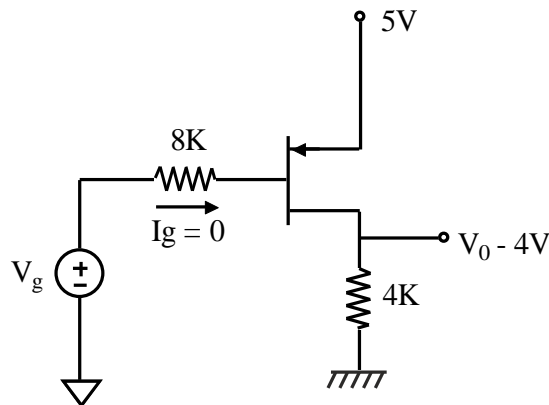# ET601M3 - Program Elective-II : CMOS Design

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Notes : 1. All questions carry marks as indicated.
         2. Assume suitable data wherever necessary.
         3. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) Compare Bipolar and MOS technology. **4**

   b) With the help of following parameters determine in which region MOSFET is working **4**
       and also find the value of drain current I_D.

   $V_{TN} = 0.8, \lambda = 0.04\,V^{-1}, Kn' = 20\,\mu A / v^2, W / L = 20, V_D = 4V, V_G = 5V \text{ and } V_s = 2V$

   c) Define Channel length modulation? Derive an expression for I_D sat along with channel **8**
       length modulation effect coefficient.

OR

2. a) How does MOS transistor acts as a switch? **4**

   b) Compare NMOS with PMOS. **4**

   c) For the PMOS circuit shown in the figure Find the value of I_D and V_{DS}; **8**
       Given $K = 0.25\,mA / v^2$; Vth = -2V

3. a) Derive an expression for CMOS inverter. **8**
       i)   Low input voltage (V_{IL})
       ii) High input voltage (V_{IH})

   b) Describe with neat diagram P-well fabrication process. **8**

OR

4.	a)	Differentiate between λ – based design rules and μ – based design rules.	**4**
	b)	Consider a CMOS inverter circuit with following parameters; $V_{DD} = 3.3V; V_{Tn} = 0.6V; V_{Tp} = -0.7V; Kn = 200\mu A / V^2; Kp = 80\mu A / V2;$ Calculate the Noise margin.	**12**
5.	a)	Explain the sources of Power dissipation in detail.	**8**
	b)	How transistor scaling is done? Discuss its effect.	**8**

OR

6.	a)	Derive an expression for short circuit dissipation for CMOS.	**8**
	b)	How Resistance, Capacitance and Inductance are computed in interconnect modeling.	**8**
7.		Design a CMOS logic circuit for the following Boolean functions.	**16**

    i) $Y = A.(B+C)+CD$

    ii) $Y = \overline{(A+B+C+D)}$

    iii) $Y = (A+B).C+D$

OR

8.	a)	What is dynamic CMOS? Explain its pre charging and evaluation mode.	**6**
	b)	Design AND gate and NOT gate with the use of stick diagram and physical layout structure.	**10**
9.	a)	Design CMOS S-R Latch by using NOR gate and NAND gate.	**8**
	b)	Explain in detail dual edge triggered flip-flop.	**8**

OR

10.	a)	Describe resettable latches and flip-flop in detail.	**8**
	b)	Implement CMOS D-Latch using proper schematic diagram.	**8**

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